CLAIMS

What is claimed is:

1. A computer system, comprising:

a processor;

a system memory coupled to said processor;

a bridge logic device coupled to said processor and said system memory and having a peripheral bus interface;

a peripheral bus comprising a plurality of address lines and coupled to the peripheral bus interface of said bridge logic device, said peripheral bus capable of coupling together various peripheral devices;

a keyboard coupled to said bridge logic device; and

a logic device coupled to said peripheral bus that swaps two address lines when a peripheral bus cycle is run to a particular asserted address line.

2. The computer system of claim 1 wherein said peripheral bus comprises a PCI bus.

3. The computer system of claim 1 wherein said logic device comprises a PLD.

4. The computer system of claim 1 wherein said logic device swaps the two address lines when a peripheral bus configuration cycle is run.

5. The computer system of claim 4 wherein said logic device issues a retry to said bridge logic which, in response, issues a retry t said processor.

6. The computer system of claim 4 wherein said peripheral bus comprises a PCI bus and said logic device is a programmable logic device that detects a PCI configuration cycle run for one of the address lines comprising the PCI bus.

7. The computer system of claim 6 further comprising an electronically controlled switch coupled to and controlled by said programmable logic device, said switch receiving two PCI bus address lines.

8. The computer system of claim 6 wherein said programmable logic device switches the two PCI bus address lines when the programmable logic device detects a PCI bus configuration cycle targeted for one the two address lines so that the address line targeted by the PCI bus configuration cycle is electrically connected to the other of said two address lines.

9. The computer system of claim 7 further including a PCI device connected to said PCI bus that has its IDSEL input pin connected to one of said two address lines.

10. The computer system of claim 1 wherein said logic device swaps the two address lines only during a portion of the peripheral bus cycle and swaps the address lines back to their original state for the rest of the bus cycle.

11. A programmable logic device coupled to a system bus comprising a plurality of address lines, said programmable logic device having logic that detects configuration read or write cycle to

a particular system bus address line and, upon detecting a configuration read or write cycle to that particular address line, the programmable logic device asserts a control signal to an electronically-controlled switch to connect the particular system bus address line to another address line.

12. The programmable logic device of claim 11 wherein said programmable logic is coupled to a PCI bus comprising a plurality of AD lines and said programmable logic device detects a PCI bus configuration read or write cycle to AD16.

13. The programmable logic device of claim 11 wherein said programmable logic is coupled to a PCI bus comprising a plurality of AD lines and said programmable logic device asserts the control signal during a portion of said configuration cycle and deasserts the control signal during the rest of the configuration cycle.

14. The programmable logic device of claim 11 wherein programmable logic device issues a retry signal upon detecting the configuration read or write cycle to the said particular address line.

15. A method of avoiding a conflict on a system bus having a plurality of address lines during a configuration cycle, comprising:

(a) detecting a configuration cycle associated with a particular system bus address line;

(b) changing the state of a switch so that one of said address lines is connected to another of said address lines; and

(c) changing the state of the switch back to its state before (b) was performed.

16. The method of claim 15 wherein the system bus comprises a PCI bus and (a) comprises detecting a PCI bus configuration cycle associated one of said PCI bus address lines.

17. The method of claim 16 wherein (b) includes changing the state of the switch during only a portion of the PCI bus configuration cycle.

18. The method of claim 17 further including issuing a retry after detecting a configuration cycle associated with the particular system bus address line and before changing the state of the switch in (b).

19. The method of claim 15 wherein (a) includes detecting a configuration cycle associated with a system bus address line that conflicts with a configuration cycle intended for a device connected to said system bus.

20. The method of claim 15 in which (b) includes connecting an address line that is not hardwired as a chip select signal to an address line that is hardwired as a chip select signal.

21. The method of claim 15 wherein (b) occurs only during an address phase of the configuration cycle.

22. The method of claim 21 wherein the system bus is a PCI bus having address lines AD[31::0] and (b) includes connecting AD16 to AD11.

23. A computer system, comprising:

a processor;

a bridge logic device coupled to said process and a system bus that comprises a plurality of address lines;

at least one system bus peripheral device connected to said system bus;

an electronically-controlled switch connected to at least one of said system bus address lines; and

a means for detecting a system bus configuration cycle associated with a certain system bus address line and, upon detecting the configuration cycle associated with the certain system bus address line, asserting a control signal to said switch to connect the certain system bus address line to another of the system bus address lines.